NCP1081

Integrated High Power PoE-PD Interface & DC-DC Converter Controller

ON Semiconductor®

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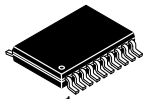

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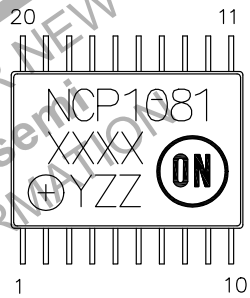

NCP1081 = Specific Device Code
XXXX = Date Code
Y = Assembly Location
ZZ = Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Introduction

The NCP1081 is a member of ON Semiconductor's high power HIPO Power over Ethernet Powered Device (PoE−PD) product family and represents a robust, flexible and highly integrated solution targeting demanding medium and high power Ethernet applications. It combines in a single unit an enhanced PoE−PD interface supporting the IEEE802.3af and the 802.3at standard and a flexible and configurable DC−DC converter controller.

The NCP1081's exceptional capabilities offer new opportunities for the design of products powered directly over Ethernet lines, eliminating the need for local power adaptors or power supplies and drastically reducing the overall installation and maintenance cost.

ON Semiconductor's unique manufacturing process and design enhancements allow the NCP1081 to deliver up to 25.5 W for the IEEE802.3at standard and up to 40 W for proprietary high power PoE applications. The NCP1081 enables the IEEE802.3at and implements a two event physical layer classification. Additional proprietary classification procedures support high power power sourcing equipment (PSE) on the market. The unique high power features leverage the significant cost advantages of PoE− enabled systems to a much broader spectrum of products in emerging markets such as industrial ethernet devices, PTZ and Dome IP cameras, RFID readers, MIMO WLAN access points, high end VoIP phones, notebooks, etc.

The integrated current mode DC−DC controller facilitates isolated and non−isolated fly−back, forward and buck converter topologies. It has all the features necessary for a flexible, robust and highly efficient design including programmable switching frequency, duty cycle up to 80 percent, slope compensation, and soft start−up.

The NCP1081 is fabricated in a robust high voltage process and integrates a rugged vertical N−channel DMOS with a low loss current sense technique suitable for the most demanding environments and capable of withstanding harsh environments such as hot swap and cable ESD events.

The NCP1081 complements ON Semiconductor's ASSP portfolio in industrial devices and can be combined with stepper motor drivers, CAN bus drivers and other high−voltage interfacing devices to offer complete solutions to the industrial and security market.

Features

- These are Pb−Free Devices

Powered Device Interface

- Supporting the IEEE802.3af and the 802.3at Standard
- Supports IEEE802.3at Two Event Layer 1 Classification
- High Power Layer 1 Classification Indicator
- Extended Power Ranges up to 40 W
- Programmable Classification Current
- Adjustable Under Voltage Lock Out
- Programmable Inrush Current Limit
- Programmable Operational Current Limit up to 1100 mA for Extended Power Ranges
- Over−temperature Protection
- Industrial Temperature Range −40°C to 85°C with Full Operation up to 150°C Junction Temperature
- 0.6 Ω Hot−swap Pass−switch with Low Loss Current Sense Technique
- Vertical N−channel DMOS Pass−switch offers the Robustness of Discrete MOSFETs with Integrated Temperature Control

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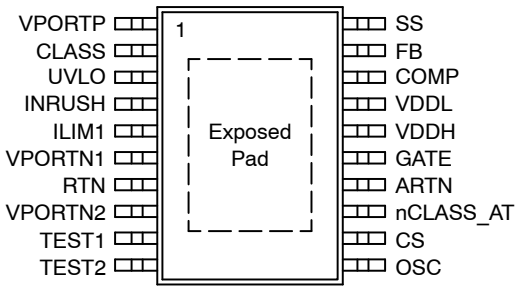
DC−DC Converter Controller

- Current Mode Control
- Supports Isolated and Non−isolated DC−DC Converter Applications
- Internal Voltage Regulators
- Wide Duty Cycle Range with Internal Slope Compensation Circuitry
- Programmable Oscillator Frequency
- Programmable Soft−start Time

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

Part Number	Package	Shipping Configuration†	Temperature Range
NCP1081DEG	TSSOP−20 EP (Pb−Free)	74 units / Tube	−40°C to 85°C
NCP1081DER2G	TSSOP−20 EP (Pb−Free)	2500 / Tape & Reel	−40°C to 85°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

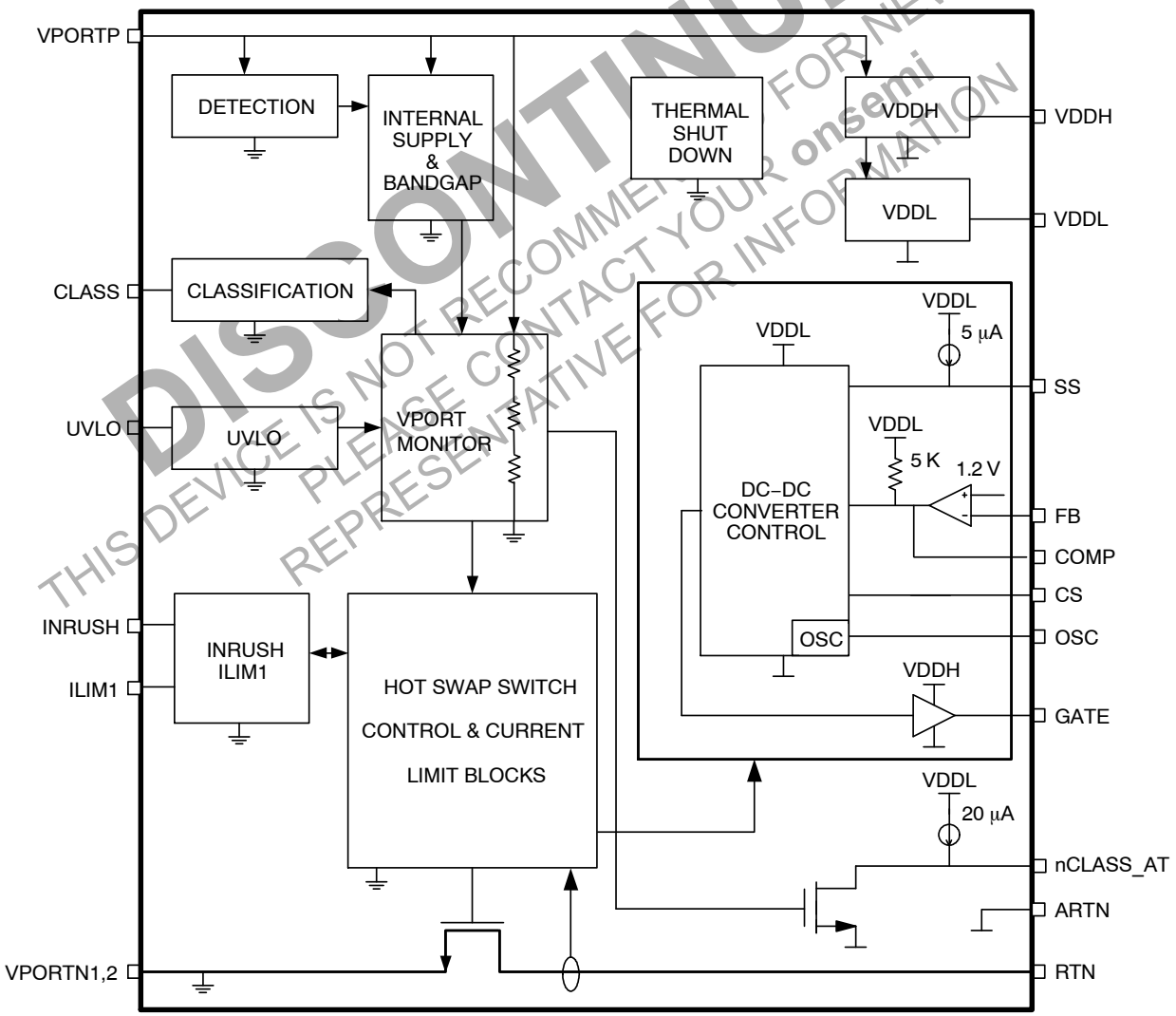


Figure 1. NCP1081 Block Diagram

SIMPLIFIED APPLICATION DIAGRAMS

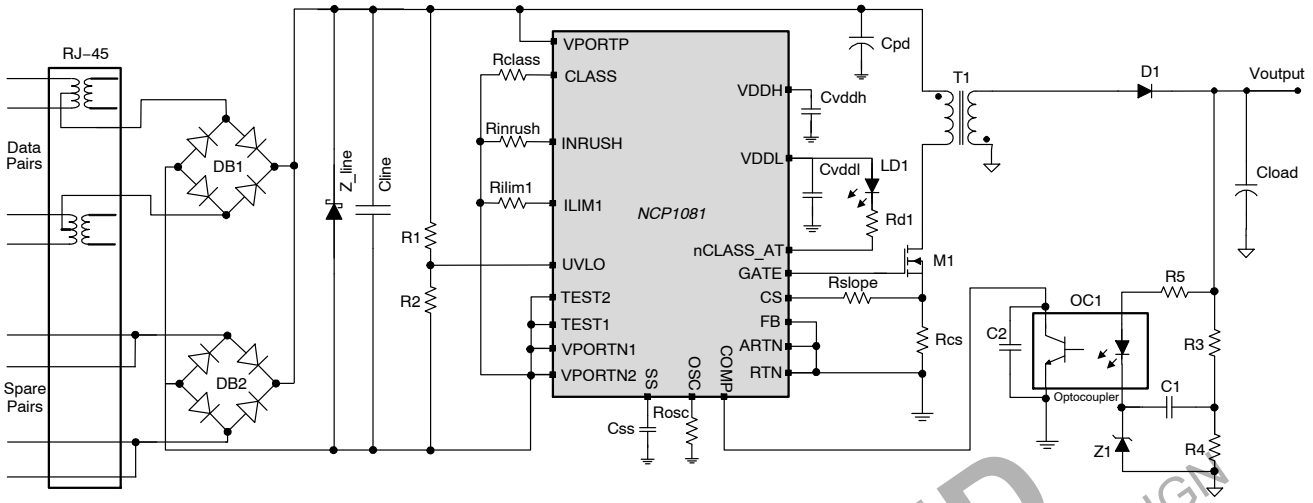


Figure 2. Isolated Fly−back Converter

Figure 2 shows the integrated PoE−PD switch and DC−DC controller configured to work in a fully isolated application. The output voltage regulation is accomplished with an external opto−coupler and a shunt regulator (Z1).

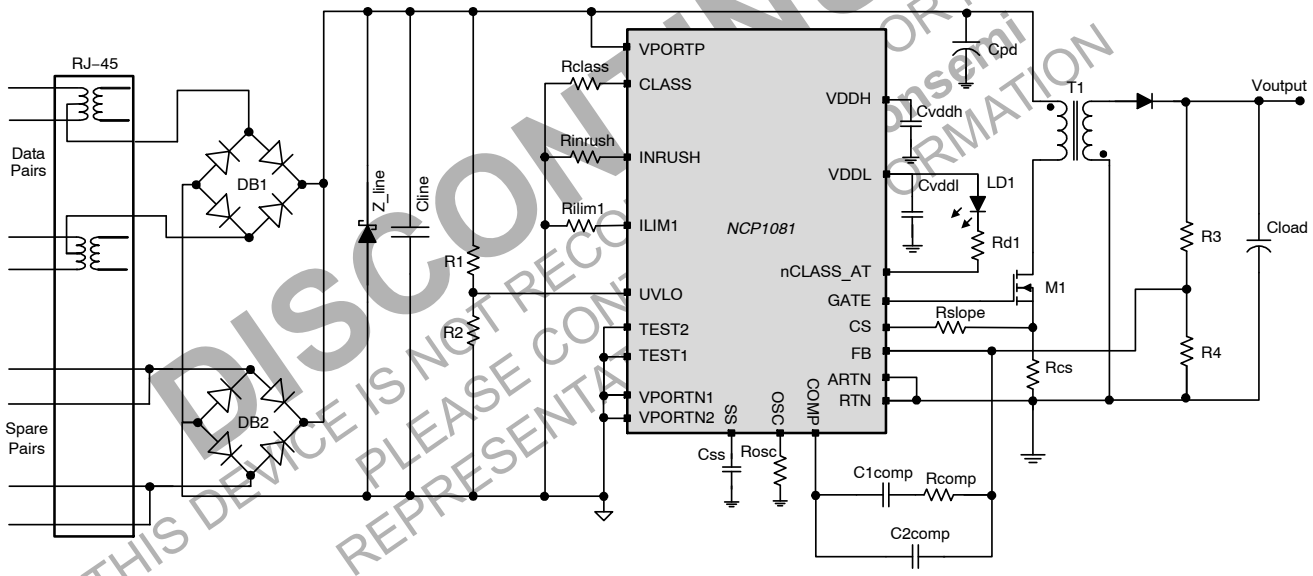


Figure 3. Non−Isolated Fly−back Converter

Figure 3 shows the integrated PoE−PD and DC−DC controller configured in a non−isolated fly−back configuration. A compensation network is inserted between the FB and the COMP pin for overall stability of the feedback loop.

SIMPLIFIED APPLICATION DIAGRAMS

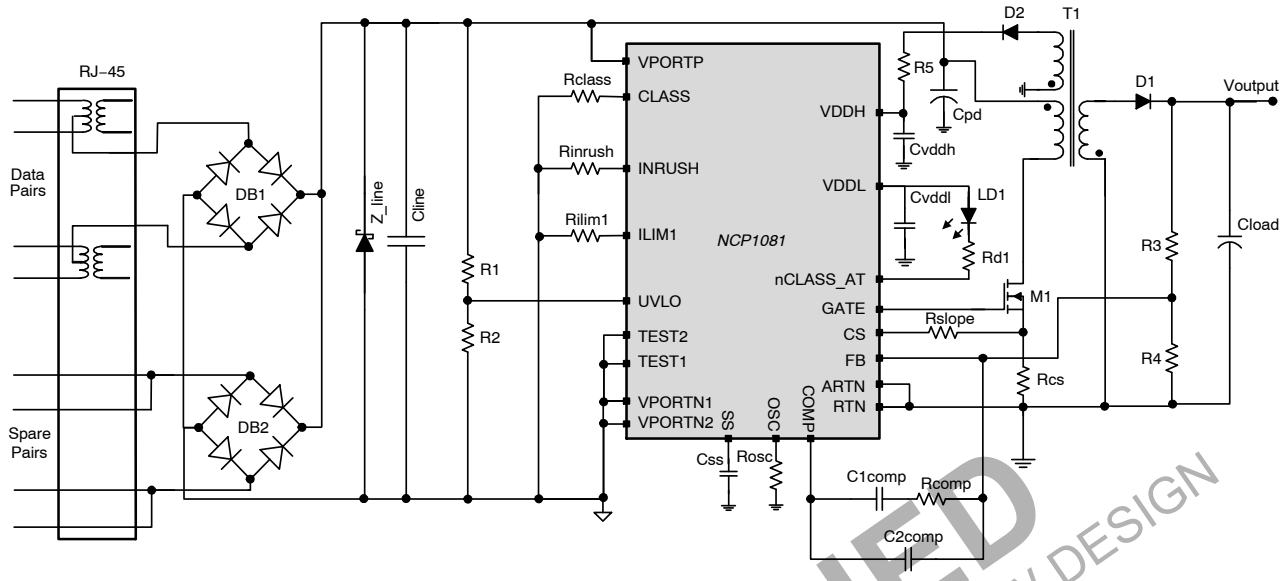


Figure 4. Non−Isolated Fly−back with Extra Winding

Figure 4 shows the same non−isolated fly−back configuration as Figure 3, but adds a 12 V auxiliary bias winding on the transformer to provide power to the NCP1081 DC−DC controller via its VDDH pin. This topology shuts off the current flowing from VPORTP to VDDH and therefore reduces the internal power dissipation of the PD, resulting in higher overall power efficiency.

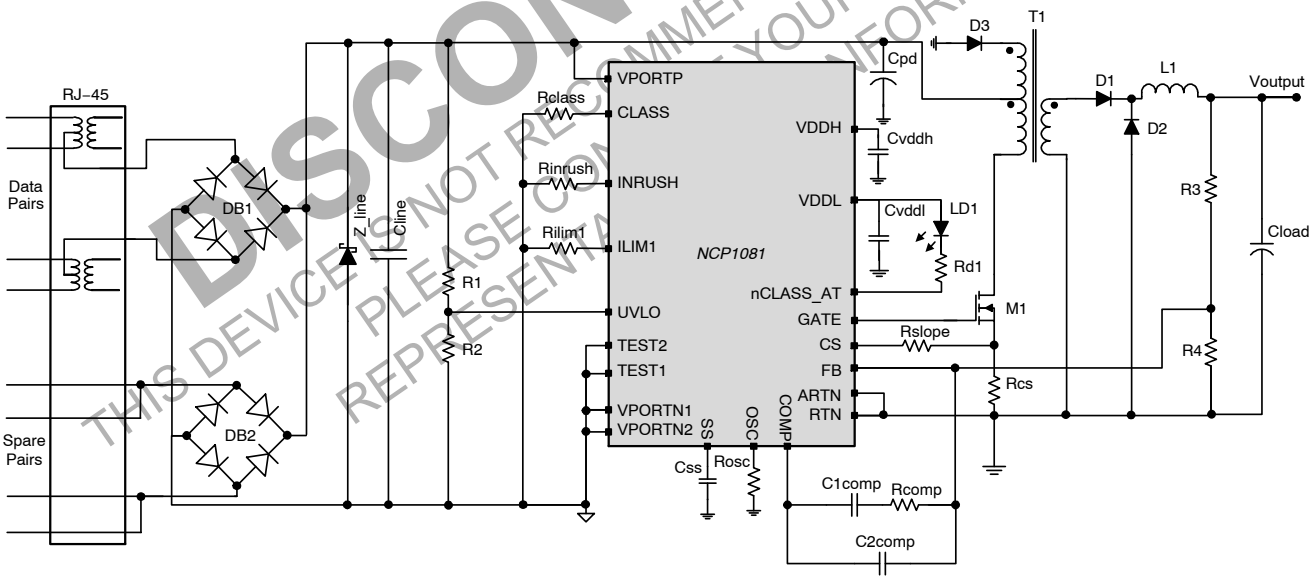


Figure 5. Non−Isolated Forward Converter

Figure 5 shows the NCP1081 used in a non−isolated forward topology.

High Power Considerations

The NCP1081 is designed to implement various configurations of high−power PoE systems including those based on the IEEE802.3at standard. High power operation can be enabled by a Dual Event Layer 1 classification or a Single Event Layer 1 classification combined with a Layer 2 high power classification. The NCP1081 also supports proprietary designs capable of delivering 25 W to 40 W to the load in two−pair configurations. A separate application note describes these implementations (AND8332).

Table 1. PIN DESCRIPTIONS

Name	Pin No.	Type	Description
VPORTP	1	Supply	Positive input power. Voltage with respect to $VPORTN_{1,2}$.
VPORTN1 VPORTN2	6,8	Ground	Negative input power. Connected to the source of the internal pass−switch.
RTN	7	Ground	DC−DC controller power return. Connected to the drain of the internal pass−switch. It must be connected to ARTN. This pin is also the drain of the internal pass−switch.
ARTN	14	Ground	DC−DC controller ground pin. Must be connected to RTN as a single point ground connection for improved noise immunity.
VDDH	16	Supply	Output of the 9 V LDO internal regulator. Voltage with respect to ARTN. Supplies the internal gate driver. VDDH must be bypassed to ARTN with a 1 μF or 2.2 μF ceramic capacitor with low ESR.
VDDL	17	Supply	Output of the 3.3 V LDO internal regulator. Voltage with respect to ARTN. This pin can be used to bias an external low−power LED (1 mA max.) connected to nCLASS_AT, and can also be used to add extra biasing current in the external opto−coupler. VDDL must be bypassed to ARTN with a 330 nF or 470 nF ceramic capacitor with low ESR.
CLASS	2	Input	Classification current programming pin. Connect a resistor between CLASS and $VPORTN_{1,2}$.
INRUSH	4	Input	Inrush current limit programming pin. Connect a resistor between INRUSH and $VPORTN_{1,2}$.
ILIM1	5	Input	Operational current limit programming pin. Connect a resistor between ILIM1 and $VPORTN_{1,2}$.
UVLO	3	Input	DC−DC controller under−voltage lockout input. Voltage with respect to $VPORTN_{1,2}$. Connect a resistor−divider from VPORTP to UVLO to $VPORTN_{1,2}$ to set an external UVLO threshold.
GATE	15	Output	DC−DC controller gate driver output pin.
OSC	11	Input	Internal oscillator frequency programming pin. Connect a resistor between OSC and ARTN.
nCLASS_AT	13	Output, Open Drain	Active−low, open−drain Layer 1 dual−finger classification indicator.
COMP	18	I/O	Output of the internal error amplifier of the DC−DC controller. COMP is pulled−up internally to VDDL with a 5 kΩ resistor. In isolated applications, COMP is connected to the collector of the opto−coupler. Voltage with respect to ARTN.
FB	19	Input	DC−DC controller inverting input of the internal error amplifier. In isolated applications, the pin should be strapped to ARTN to disable the internal error amplifier.
CS	12	Input	Current−sense input for the DC−DC controller. Voltage with respect to ARTN.
SS	20	Input	Soft−start input for the DC−DC controller. A capacitor between SS and ARTN determines the soft−start timing.
TEST1	9	Input	Digital test pin must always be connected to $VPORTN_{1,2}$.
TEST2	10	Input	Digital test pin must always be connected to $VPORTN_{1,2}$.
EP			Exposed pad. Connected to $VPORTN_{1,2}$ ground.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Units	Conditions
VPORTP	Input power supply	−0.3	72	V	Voltage with respect to $VPORTN_{1,2}$
RTN ARTN	Analog ground supply 2	−0.3	72	V	Pass−switch in off−state (Voltage with respect to $VPORTN_{1,2}$)
VDDH	Internal regulator output	−0.3	17	V	Voltage with respect to ARTN
VDDL	Internal regulator output	−0.3	3.6	V	Voltage with respect to ARTN
CLASS	Analog output	−0.3	3.6	V	Voltage with respect to $VPORTN_{1,2}$
INRUSH	Analog output	−0.3	3.6	V	Voltage with respect to $VPORTN_{1,2}$
ILIM1	Analog output	−0.3	3.6	V	Voltage with respect to $VPORTN_{1,2}$
UVLO	Analog input	−0.3	3.6	V	Voltage with respect to $VPORTN_{1,2}$
OSC	Analog output	−0.3	3.6	V	Voltage with respect to ARTN
COMP	Analog input / output	−0.3	3.6	V	Voltage with respect to ARTN
FB	Analog input	−0.3	3.6	V	Voltage with respect to ARTN
CS	Analog input	−0.3	3.6	V	Voltage with respect to ARTN
SS	Analog input	−0.3	3.6	V	Voltage with respect to ARTN
nCLASS_AT	Analog output	−0.3	3.6	V	Voltage with respect to ARTN
TEST1 TEST2	Digital inputs	−0.3	3.6	V	Voltage with respect to $VPORTN_{1,2}$
Ta	Ambient temperature	−40	85	°C	
Tj	Junction temperature	−	150	°C	
Tj−TSD	Junction temperature (Note 1)	−	175	°C	Thermal shutdown condition
T_{stg}	Storage Temperature	−55	150	°C	
$T_{\theta JA}$	Thermal Resistance, Junction to Air (Note 2)		37.6	°C/W	Exposed pad connected to $VPORTN_{1,2}$ ground
ESD−HBM	Human Body Model	4	−	kV	per JEDEC Standard JESD22
ESD−CDM	Charged Device Model	750	−	V	
ESD−MM	Machine Model	300	−	V	
LU	Latch−up	±200	−	mA	per JEDEC Standard JESD78
ESD−SYS	System ESD (contact/air) (Note 3)	8/15	−	kV	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tj−TSD allowed during error conditions only. It is assumed that this maximum temperature condition does not occur more than 1 hour cumulative during the useful life for reliability reasons.
2. Mounted on a 1S2P (3 layer) test board with copper coverage of 25 percent for the signal layers and 90 percent copper coverage for the inner planes at an ambient temperature of 85°C in still air. Refer to JEDEC JESD51−7 for details.
3. Surges per EN61000−4−2, 1999 applied between RJ−45 and output ground and between adapter input and output ground of the evaluation board. The specified values are the test levels and not the failure levels.

Recommended Operating Conditions

Operating conditions define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating conditions described in this section is not warranted. Operating outside the recommended operating conditions for extended periods of time may affect device reliability.

All values concerning the DC−DC controller, VDDH, VDDL, and nCLASS_AT blocks are with respect to ARTN. All others are with respect to $VPORTN_{1,2}$ (unless otherwise noted).

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT SUPPLY						
VPORT	Input supply voltage	0		57	V	VPORT = VPORTP – $VPORTN_{1,2}$
SIGNATURE DETECTION						
Vsignature	Input supply voltage signature detection range	1.4		9.5	V	
Rsignature	Signature resistance (Note 4)	23.75		26.25	kΩ	
Offset_current	I_VportP + I_Rtn	–	1.8	5	μA	VPORTP = RTN = 1.4 V
Sleep_current	I_VportP + I_Rtn	–	15	25	μA	VPORTP = RTN = 9.5 V
CLASSIFICATION						
Vcl	Input supply voltage classification range	13		20.5	V	
V_mark	Mark event voltage range (VPORTP falling)	5.4	–	9.7	V	
I_mark	Current consumption I(VPORTP) + I(Rdet) in Mark Event range	0.5	–	2.0	mA	5.4 V ≤ VPORT ≤ 9.5 V
dR_mark	Input signature during Mark Event (Note 7)	–	–	12	kΩ	For information only
Vreset	Classification Reset range (VPORTP falling)	4.3	4.9	5.4	V	
Iclass0	Class 0: Rclass 10 kΩ (Note 6)	0	–	4	mA	Iclass0 = I_VportP + I_Rdet
Iclass1	Class 1: Rclass 130 Ω (Note 6)	9	–	12	mA	Iclass1 = I_VportP + I_Rdet
Iclass2	Class 2: Rclass 69.8 Ω (Note 6)	17	–	20	mA	Iclass2 = I_VportP + I_Rdet
Iclass3	Class 3: Rclass 44.2 Ω (Note 6)	26	–	30	mA	Iclass3 = I_VportP + I_Rdet
Iclass4	Class 4: Rclass 30.9 Ω (Note 6)	36	–	44	mA	Iclass4 = I_VportP + I_Rdet
Iclass5	Class 5: Rclass 22.1 Ω (Notes 5 and 6) (for proprietary high power applications)	50	–	60	mA	Iclass5 = I_VportP + I_Rdet
IDC_{class}	Internal current consumption during classification (Note 8)	–	600	–	μA	For information only
CLASSIFICATION INDICATOR						
nCLASS_AT_i	nCLASS_AT current source	13	20	27	μA	
NCLASS_AT_pd	$R_{DS,ON}$ of NCLASS_AT pull down transistor		130		Ω	For information only

4. Test done according to the IEEE802.3af 2 Point Measurement. The minimum probe voltages measured at the PoE−PD are 1.4 V and 2.4 V, and the maximum probe voltages are 8.5 V and 9.5 V.
5. This extended classification range can be used with a PSE which also uses this classification range to deliver more current than specified by IEEE802.3.
6. Measured with an external Rdet of 25.5 kΩ between VPORTP and $VPORTN_{1,2}$, and for 13 V < VPORT < 20.5 V (with VPORT = VPORTP − $VPORTN_{1,2}$). Resistors are assumed to have 1% accuracy.
7. Measured with the 2 Point Measurement defined in the IEEE802.3af standard with 5.4 V and 9.5 V the extreme values for V2 and V1.
8. This typical current excludes the current in the Rclass and Rdet external resistors.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
UVLO						
Vuvlo_on	Default turn on voltage (VportP rising)	–	38	40	V	UVLO pin tied to $VPORTN_{1,2}$
Vuvlo_off	Default turn off voltage (VportP falling)	29.5	32	–	V	UVLO pin tied to $VPORTN_{1,2}$
Vhyst_int	UVLO internal hysteresis	–	6	–	V	UVLO pin tied to $VPORTN_{1,2}$
Vuvlo_pr	UVLO external programming range	25	–	50	V	UVLO pin connected to the resistor divider (R1 & R2). For information only
Vhyst_ext	UVLO external hysteresis	–	15	–	%	UVLO pin connected to the resistor divider (R1 & R2)
Uvlo_Filter	UVLO on/off filter time	–	90	–	μS	For information only
PASS−SWITCH AND CURRENT LIMITS						
Ron	Pass−switch Rds−on	–	0.6	1.2	Ω	Max Ron specified at Tj = 130°C
I_Rinrush1	Rinrush = 150 kΩ (Note 9)	95	125	155	mA	Measured at RTN−$VPORTN_{1,2}$ = 3 V
I_Rinrush2	Rinrush = 57.6 kΩ (Note 9)	260	310	360	mA	Measured at RTN−$VPORTN_{1,2}$ = 3 V
I_Rilim1	Rilim1 = 84.5 kΩ (Note 9)	450	510	570	mA	Current limit threshold
I_Rilim2	Rilim1 = 66.5 kΩ (Note 9)	600	645	690	mA	Current limit threshold
I_Rilim3	Rilim1 = 55.6 kΩ (Note 9)	720	770	820	mA	Current limit threshold
I_Rilim4	Rilim1 = 38.3 kΩ (Note 9)	970	1100	1230	mA	Current limit threshold
INRUSH AND ILIM1 CURRENT LIMIT TRANSITION						
Vds_pgood	VDS required for power good status	0.8	1	1.2	V	RTN−$VPORTN_{1,2}$ falling; Voltage with respect to $VPORTN_{1,2}$
Vds_pgood_hyst	VDS hysteresis required for power good status	–	8.2	–	V	Voltage with respect to $VPORTN_{1,2}$

9. The current value corresponds to the PoE−PD input current (the current flowing in the external Rdet and the quiescent current of the device are included). Resistors are assumed to have 1% accuracy.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
VDDH REGULATOR						
VDDH_reg	Regulator output voltage (Notes 10 and 11) Ivddh_load + Ivddl_load < 10 mA with 0 < Ivddl_load < 2.25 mA	8.4	9	9.6	V	
VDDH_Off	Regulator turn−off voltage	–	VDDH_reg + 0.5 V	–	V	For information only
VDDH_lim	VDDH regulator current limit (Notes 10 and 11)	13	–	26	mA	
VDDH_Por_R	VDDH POR level (rising)	7.3	–	8.3	V	
VDDH_Por_F	VDDH POR level (falling)	6	–	7	V	
VDDH_ovlo	VDDH over−voltage level (rising)	16	–	18.5	V	
VDDL REGULATOR						
VDDL_reg	Regulator output voltage (Notes 10 and 11) 0 < Ivddl_load < 2.25 mA with Ivddh_load + Ivddl_load < 10 mA	3.05	3.3	3.55	V	
VDDL_Por_R	VDDL POR level (rising)	VDDL − 0.2	–	VDDL − 0.02	V	
VDDL_Por_F	VDDL POR level (falling)	2.5	–	2.9	V	
GATE DRIVER						
Gate_Tr	GATE rise time (10−90%)	–	–	50	ns	Cload = 2 nF, VDDHreg = 9 V
Gate_Tf	GATE fall time (90−10%)	–	–	50	ns	Cload = 2 nF, VDDHreg = 9 V
PWM COMPARATOR						
VCOMP	COMP control voltage range	1.3	–	3	V	For information only
ERROR AMPLIFIER						
Vbg_fb	Reference voltage	1.15	1.2	1.25	V	Voltage with respect to ARTN
Av_ol	DC open loop gain	–	80	–	dB	For information only
GBW	Error amplifier GBW	1	–	–	MHz	For information only
SOFT−START						
Vss	Soft−start voltage range	–	1.15	–	V	
Vss_r	Soft−start low threshold (rising edge)	0.35	0.45	0.55	V	
Iss	Soft−start source current	3	5	7	μA	
CURRENT LIMIT COMPARATOR						
CSth	CS threshold voltage	324	360	396	mV	
Tblank	Blanking time	–	100	–	ns	For information only
OSCILLATOR						
DutyC	Maximum duty cycle	–	80%	–		Fixed internally
Frange	Oscillator frequency range	100	–	500	kHz	
F_acc	Oscillator frequency accuracy		±25		%	

10. Power dissipation must be considered. Load on VDDH and VDDL must be limited especially if VDDH is not powered by an auxiliary winding.
11. Ivddl_load = current flowing out of the VDDL pin.
    Ivddh_load = current flowing out of the VDDH pin + current delivered to the Gate Driver (function of the frequency, VDDH voltage & MOSFET gate capacitance).

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
CURRENT CONSUMPTION						
I_{vportP_1}	VPORTP internal current consumption (Note 12)	–	2.5	3.5	mA	DC−DC controller off
I_{vportP_2}	VPORTP internal current consumption (Note 13)	–	4.7	6.5	mA	DC−DC controller on
THERMAL SHUTDOWN						
TSD	Thermal shutdown threshold	150	–	–	°C Tj	Tj = junction temperature
Thyst	Thermal hysteresis	–	15	–	°C Tj	Tj = junction temperature
THERMAL RATINGS						
Ta	Ambient temperature	−40	–	85	°C	
Tj	Junction temperature	–	–	125 150	°C °C	Parametric values guaranteed Max 1000 hours

12. Conditions
    a. No current through the pass−switch
    b. DC−DC controller inactive (SS shorted to RTN)
    c. No external load on VDDH and VDDL
    d. VPORTP = 57 V
13. Conditions
    a. No current through the pass−switch
    b. Oscillator frequency = 100 kHz
    c. No external load on VDDH and VDDL
    d. Aux winding not used
    e. 2 nF on GATE, DC−DC controller enabled
    f. VPORTP = 57 V

DESCRIPTION OF OPERATION

Powered Device Interface

The PD interface portion of the NCP1081 supports the IEEE802.3af and 802.3at defined operating modes: detection signature, current source classification, inrush and operating current limits. In order to give more flexibility to the user and also to keep control of the power dissipation in the NCP1081, both current limits are configurable. The device enters operation once its programmable Vuvlo_on threshold is reached, and operation ceases when the supplied voltage falls below the Vuvlo_off threshold. Sufficient hysteresis and Uvlo filter time are provided to avoid false power on/off cycles due to transient voltage drops on the cable.

Detection

During the detection phase, the incremental equivalent resistance seen by the PSE through the cable must be in the IEEE802.3af standard specification range (23.75 kΩ to 26.25 kΩ) for a PSE voltage from 2.7 V to 10.1 V. In order to compensate for the non-linear effect of the diode bridge and satisfy the specification at low PSE voltage, the NCP1081 presents a suitable impedance in parallel with the 25.5 kΩ R_{det} external resistor connected between VPORTP and VPORTN. For some types of diodes (especially Schottky diodes), it may be necessary to adjust this external resistor.

When the Detection_Off level is detected (typically 11.5 V) on VPORTP, the NCP1081 turns on its internal 3.3 V regulator and biasing circuitry in anticipation of the classification phase as the next step.

Classification

Once the PSE device has detected the PD device, the classification process begins. The NCP1081 is fully capable of responding and completing all classification handshaking procedures as described next.

Classification Current Source Generation

In classification, the PD regulates a constant current source that is set by the external resistor RCLASS value on the CLASS pin. Figure 6 shows the schematic overview of the classification block. The current source is defined as:

$$I_{class} = \frac{V_{bg}}{R_{class}}, \text{ (where } V_{bg} \text{ is 1.2 V)}$$

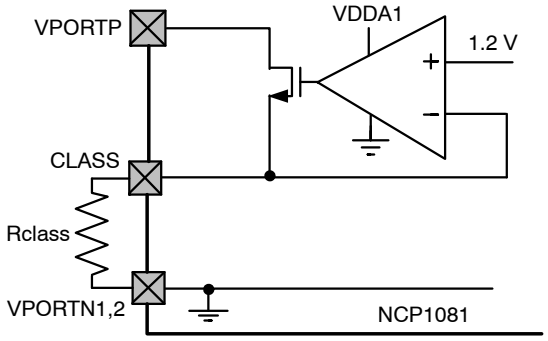


Figure 6. Classification Block Diagram

The NCP1081 can handle all defined types of classification, IEEE802.3af, 802.3at and proprietary classification.

In the IEEE802.3af standard the classification is performed with a Single Event Layer 1 classification. Depending on the current level set during that single event the power level is determined. The IEEE802.3at standard allows two ways of classification which can also be combined. These two approaches enable higher power applications through a variety of PSE equipment.

For power injectors and midspans a pure physical hardware handshake is introduced called Two Event Layer 1 classification. This approach allows equipment that has no data link between PSE and PD to classify as high power.

Since switches can establish a data link between PSE and PD, a software handshake is possible. This type of handshake is called Layer 2 classification (or Data Link Layer classification). It has the main advantage of having a finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation.

Table 4. Single and Dual Event Classification

Standard	Layer	Handshake
802.3af	1	Single event physical classification
802.3at	1	Two event physical classification
802.3at	2	Data-link (IP) communication classification

One Event Layer 1 Classification

An IEEE802.3af compliant PSE performs only One Event Layer 1 classification event by increasing the line voltage into the classification range only once.

Two Event Layer 1 Classification

A IEEE802.3at compliant PSE using this physical classification performs two classification events and looks for the appropriate response from the PD to check if the PD is IEEE802.3at compatible.

The PSE will generate the sequence described in Figure 7. During the first classification finger, the PSE will measure the classification current which should be 40 mA if the PD is at compliant. If this is the case, the PSE will exit the classification range and will force the line voltage into the Mark Event range. Within this range, the PSE may check the non-valid input signature presented by the PD (using the two point measurement defined in the IEEE802.3af standard). Then the PSE will repeat the same sequence with the second classification finger. A PD which has detected the sequence "***Finger + Mark + Finger + Mark***" knows the PSE is IEEE802.3at compliant, meaning the PSE will deliver more current on the port. (Note that a PSE IEEE802.3at compliant may apply more than two fingers, but the final result will be the same as two fingers).

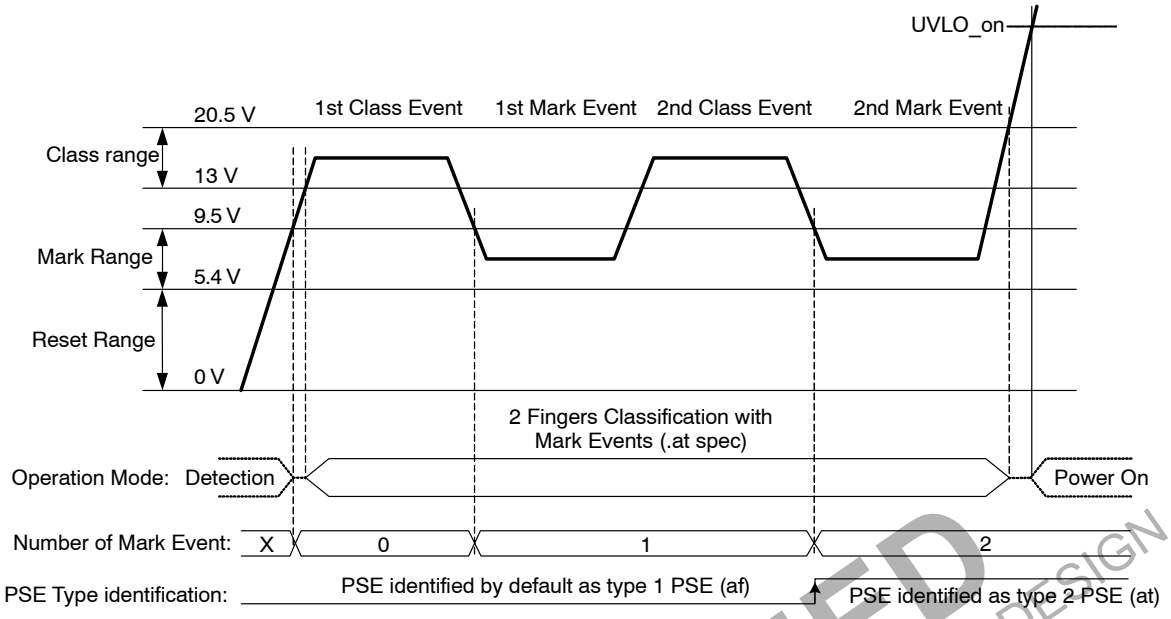


Figure 7. Hardware Physical Classification Event Sequence

nCLASS_AT Indicator

The nCLASS_AT active low open drain output pin can be used to notify to the microprocessor of the powered device that the PSE performed a one or two event hardware classification. If a two event hardware classification has occured and once the PD application is supplied power by the NCP1081 DC-DC converter, the nCLASS_AT pin will be pulled down to ARTN by the internal low voltage NMOS switch (ARTN is the ground connection of the DC-DC converter). Otherwise, nCLASS_AT will be disabled and will be pulled up to VDDL (3.3 V typ) via an internal current source (20 μA typ) and via the external pull-up resistor.

The following scheme illustrates how the nCLASS_AT pin may be configured with the processor of the powered device. An opto-coupler is used to guarantee full isolation between the Ethernet cable and the application.

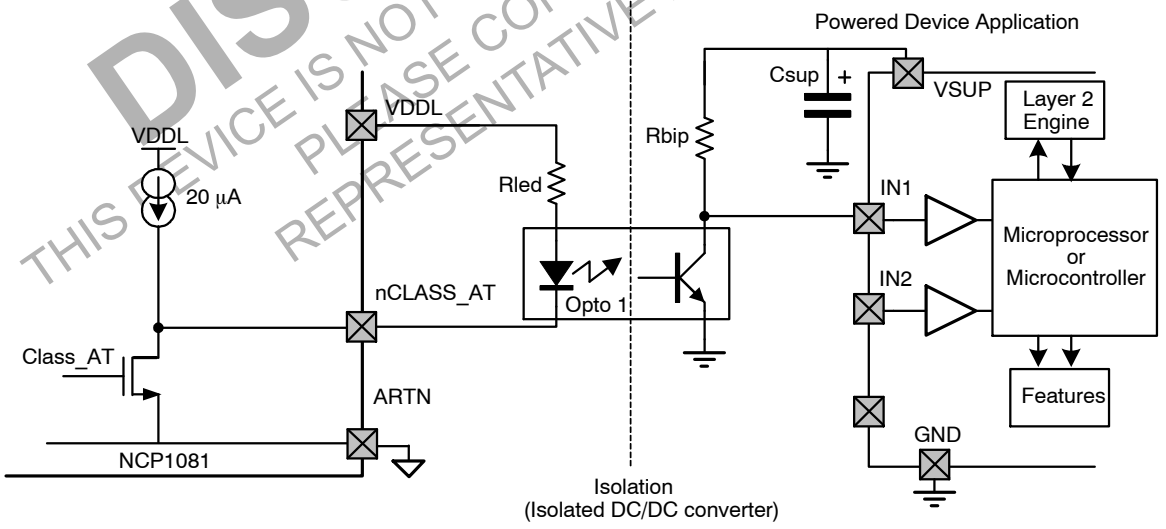


Figure 8. Isolated nClass_AT Communication with the Powered Device Application

As soon as the application is powered by the DC-DC converter and completes initialization, the microprocessor should check if the NCP1081 detected a two event hardware classification by reading its digital input (pin IN1 in this example). If pin IN1 is low, the application knows power is supplied by a IEEE802.3at compliant PSE, and can deliver power up to the level specified by the IEEE802.3at standard.

Otherwise the application will have to perform a Layer 2 classification with the PSE. There are several scenarios for which the NCP1081 will not enable its nCLASS_AT pin:

- The PSE skipped the classification phase.
- The PSE performed a one event hardware classification (it can be a IEEE802.3af or a 802.3at compliant PSE with Layer 2 engine).
- The PSE performed a two event hardware classification but it did not properly control the input voltage in the mark voltage window, (for example it crossed the reset range).

Power Mode

When the classification hand−shake is completed, the PSE and PD devices move into the operating mode.

Under Voltage Lock Out (UVLO)

The NCP1081 incorporates an under voltage lock out (UVLO) circuit which monitors the input voltage and determines when to apply power to the DC−DC controller.

To use the default settings for UVLO (see Table 3), the pin UVLO must be connected to $VPORTN_{1,2}$. In this case the signature resistor has to be placed directly between VPORTP and $VPORTN_{1,2}$, as shown in Figure 9.

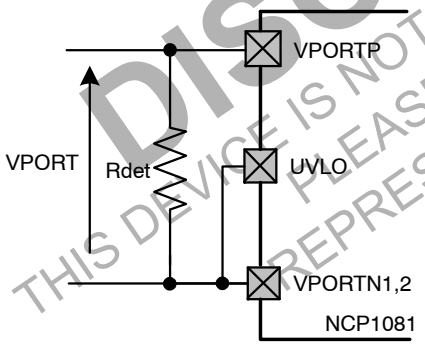


Figure 9. Default UVLO Settings

To define the UVLO threshold externally, the UVLO pin must be connected to the center of an external resistor divider between VPORTP and $VPORTN_{1,2}$ as shown in Figure 10. The series resistance value of the external resistors must add to 25.5 kΩ and replaces the internal signature resistor.

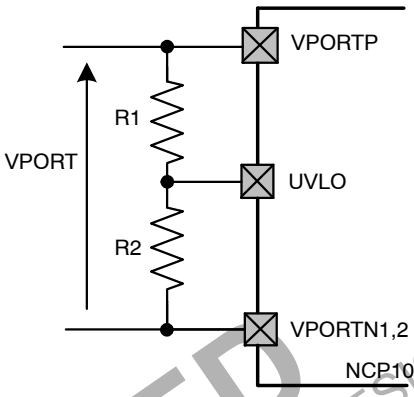


Figure 10. External UVLO Configuration

For a Vuvlo_on desired turn−on voltage threshold, R1 and R2 can be calculated using the following equations:

$$R1 + R2 = R_{det}$$

$$R2 = \frac{1.2}{V_{ulvo\_on}} \times R_{det}$$

When using the external resistor divider, the NCP1081 has an external reference voltage hysteresis of 15 percent typical.

Inrush and Operational Current Limitations

The inrush current limit and the operational current limit are programmed individually by an external Rinrush and Rilim1 resistors respectively connected between INRUSH and $VPORTN_{1,2}$, and between ILIM1 and $VPORTN_{1,2}$ as shown in Figure 11.

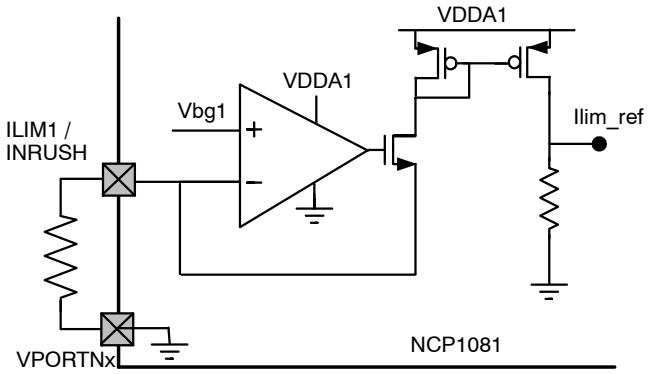


Figure 11. Current Limitation Configuration (Inrush & Ilim1 Pins)

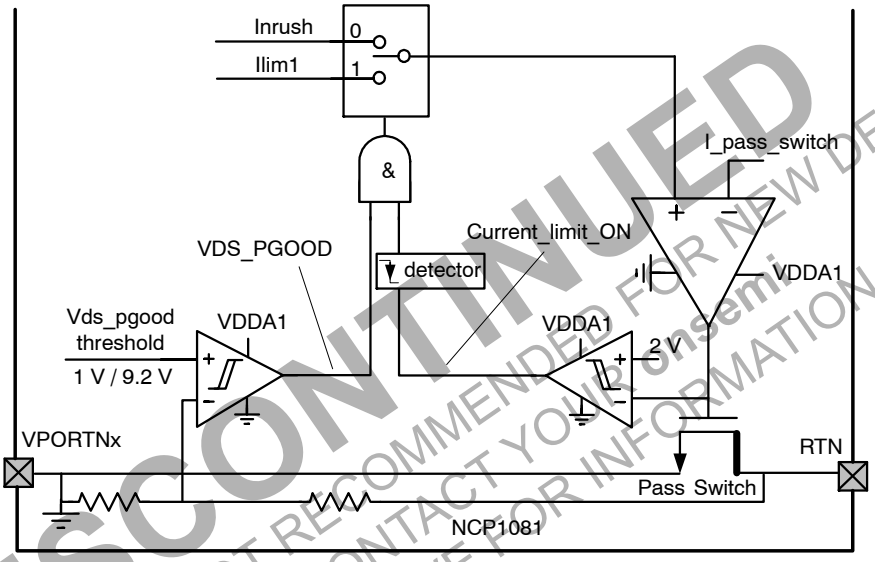


Figure 12. Inrush and Ilim1 Selection Mechanism

When VPORT reaches the UVLO_on level, the Cpd capacitor is charged with the INRUSH current (in order to limit the internal power dissipation of the pass−switch). Once the Cpd capacitor is fully charged, the current limit switches from the inrush current to the current limit level (ilim1) as shown in Figure 12. This transition occurs when both following conditions are satisfied:

1. The VDS of the pass−switch is below the Vds_pgood low level (1 V typical).
2. The pass−switch is no longer in current limit mode, meaning the gate of the pass−switch is “high” (above 2 V typical).

The operational current limit will stay selected as long as Vds_pgood is true (meaning that RTN−$VPORTN_{1,2}$ is below the high level of Vds_pgood). This mechanism allows a current level transition without any current spike in the pass−switch because the operational current limit (ilim1) is enabled once the pass−switch is not limiting the current anymore, meaning that the Cpd capacitor is fully charged.

Thermal Shutdown

The NCP1081 includes thermal protection which shuts down the device in case of high power dissipation. Once the thermal shutdown (TSD) threshold is exceeded, following blocks are turned off:

- DC−DC controller
- Pass−switch
- VDDH and VDDL regulators
- CLASS regulator

When the TSD error disappears and if the input line voltage is still above the UVLO level, the NCP1081 automatically restarts with the current limit set in the inrush state, the DC−DC controller is disabled and the Css (soft−start capacitor) discharged. The DC−DC controller becomes operational as soon as capacitor Cpd is fully charged.

DC−DC Converter Controller

The NCP1081 implements a current mode DC−DC converter controller which is illustrated in Figure 13.

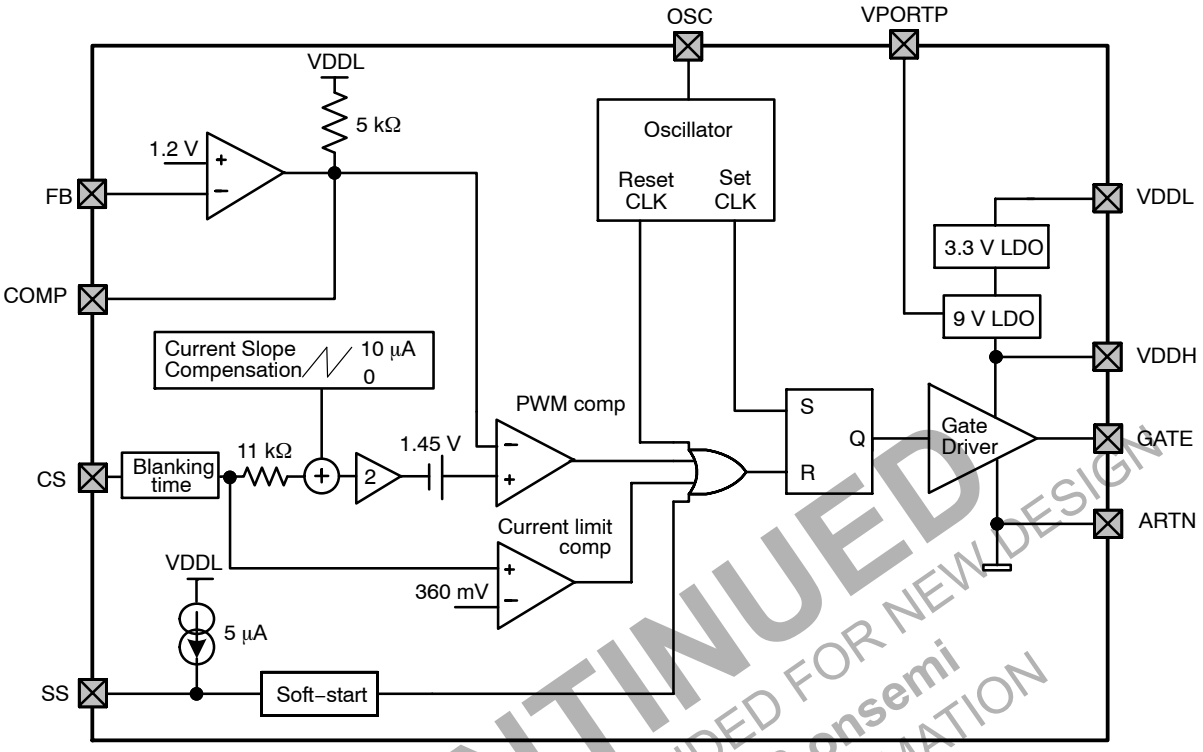


Figure 13. DC−DC Controller Block Diagram

Internal VDDH and VDDL Regulators and Gate Driver

An internal linear regulator steps down the VPORTP voltage to a 9 V output on the VDDH pin. VDDH supplies the internal gate driver circuit which drives the GATE pin and the gate of the external power MOSFET. The NCP1081 gate driver supports an external MOSFET with high Vth and high input gate capacitance. A second LDO regulator steps down the VDDH voltage to a 3.3 V output on VDDL. VDDL powers the analog circuitry of the DC-DC controller and nCLASS_AT blocks. Moreover it can provide current to light a LED connected on the nCLASS_AT pin.

In order to prevent uncontrolled operations, both regulators include power−on−reset (POR) detectors which prevent the DC−DC controller from operating when either VDDH or VDDL is too low. In addition, an over−voltage lockout (OVLO) on the VDDH supply disables the gate driver in case of an open−loop converter with a configuration using the bias winding of the transformer (see Figure 4).

Both VDDH and VDDL regulators turn on as soon as VPORT reaches the Vuvlo_on threshold.

Error Amplifier

In non−isolated converter topologies, the high gain internal error amplifier of the NCP1081 and the internal 1.2 V reference voltage regulate the DC−DC output voltage. In this configuration, the feedback loop compensation network should be inserted between the FB and COMP pins as shown in Figures 3, 4 and 5.

In isolated topologies the error amplifier is not used because it is already implemented externally with the shunt regulator on the secondary side of the DC−DC controller (see Figure 2). Therefore the FB pin must be strapped to ARTN and the output transistor of the opto−coupler has to be connected on the COMP pin where an internal 5 kΩ pull−up resistor is tied to the VDDL supply (see Figure 13).

Soft−Start

The soft−start function provided by the NCP1081 allows the output voltage to ramp up in a controlled fashion, eliminating output voltage overshoot. This function is programmed by connecting a capacitor C_{SS} between the SS and ARTN pins.

While the DC−DC controller is in POR, the capacitor C_{SS} is fully discharged. After coming out of POR, an internal current source of 5 μA typically starts charging the capacitor C_{SS} to initiate soft−start. When the voltage on SS pin has reached 0.45 V (typical), the gate driver is enabled and DC−DC operation starts with a duty cycle limit which increases with the SS pin voltage. The soft−start function is finished when the SS pin voltage goes above 1.6 V for which the duty cycle limit reaches its maximum value of 80 percent.

Soft−start can be programmed by using the following equation:

$$t_{SS}(ms) = 0.23 \times C_{SS}(nF)$$

Current Limit Comparator

The NCP1081 current limit block behind the CS pin senses the current flowing in the external MOSFET for current mode control and cycle−by−cycle current limit. This is performed by the current limit comparator which, on the CS pin, senses the voltage across the external Rcs resistor located between the source of the MOSFET and the ARTN pin.

The NCP1081 also provides a blanking time function on CS pin which ensures that the current limit and PWM comparators are not prematurely trigged by the current spike that occurs when the switching MOSFET turns on.

Slope Compensation Circuitry

To overcome sub−harmonic oscillations and instability problems that exist with converters running in continuous conduction mode (CCM) and when the duty cycle is close or above 50 percent, the NCP1081 integrates a current slope compensation circuit. The amplitude of the added slope compensation is typically 110 mV over one cycle.

As an example, for an operating switching frequency of 250 kHz, the internal slope provided by the NCP1081 is 27.5 mV/ μA typically.

DC−DC Controller Oscillator

The frequency is configured with the Rosc resistor inserted between OSC and ARTN, and is defined by the following equation:

$$R_{OSC}(k\Omega) = \frac{38600}{F_{OSC}(kHz)}$$

The duty cycle limit is fixed internally at 80 percent.

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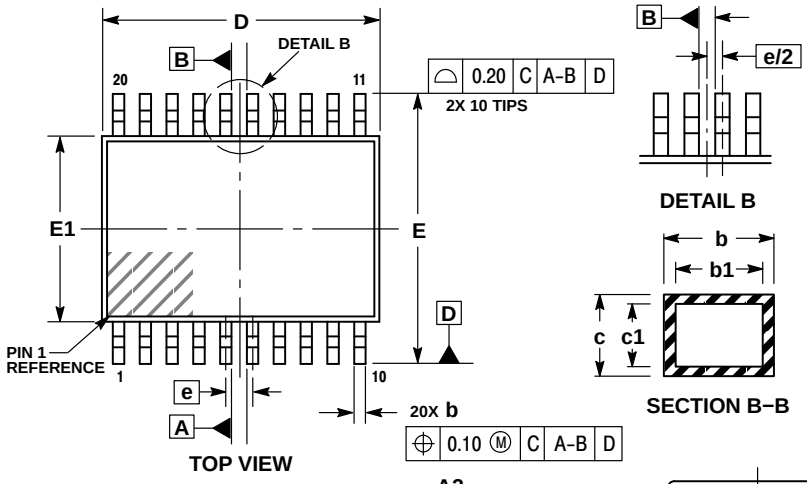
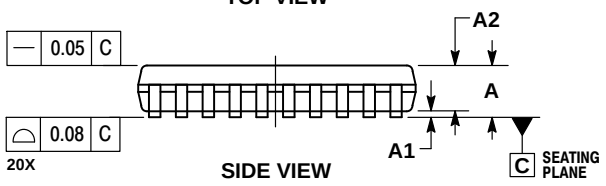
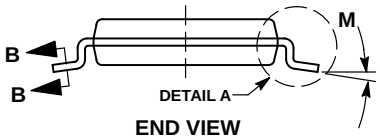
CASE 948AB
ISSUE O

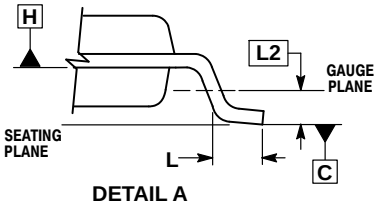
DATE 17 JUN 2008

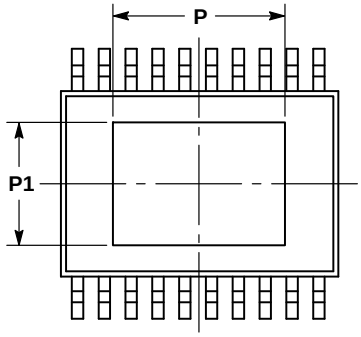
SCALE 1:1



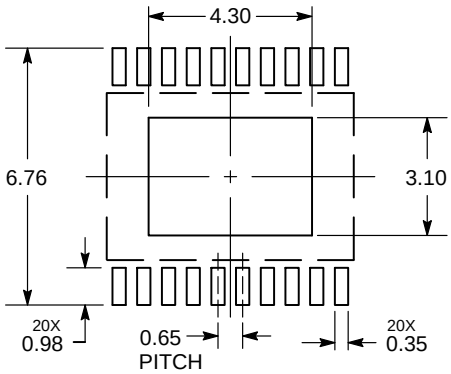








SOLDERING FOOTPRINT

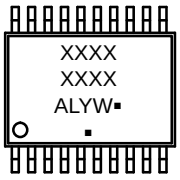


DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07 IN EXCESS OF THE LEAD WIDTH AT MMC. DAMBAR CANNOT BE LOACTED ON THE LOWER RADIUS OR THE FOOT OF THE LEAD.
4. DIMENSIONS b, b1, c, c1 TO BE MEASURED BETWEEN 0.10 AND 0.25 FROM LEAD TIP.
5. DATUMS A AND B ARE ARE DETERMINED AT DATUM H. DATUM H IS LOACTED AT THE MOLD PARTING LINE AND COINCIDENT WITH LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
6. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.10
A1	0.05	0.15
A2	0.85	0.95
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	6.40	6.60
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.70
L2	0.25 BSC	
M	0°	8°
P	---	4.20
P1	---	3.00

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

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